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SUN MICROSYSTEMS/FINNEGAN, HENDERSON LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
NGO, CHUONG D	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/035,579
Filing Date: December 28, 2001
Appellant(s): STEELE, GUY L.

Nathan A. Sloan
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 04/07/2006 appealing from the Office action mailed 05/25/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The Appeal of U.S. Patent Application No. 10/035,747.

The Appeal of U.S. Patent Application No. 10/035,595.

The Appeal of U.S. Patent Application No. 10/035,584.

The Appeal of U.S. Patent Application No. 10/035,587.

The Appeal of U.S. Patent Application No. 10/035,647.

The Appeal of U.S. Patent Application No. 10/035,580.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,009,511	LYNCH et al.	12-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch et al. (6,009,511).

As per claim 1,5,14,18,26 and 30, Lynch et al. discloses in figure 1 a floating point system (36) for performing floating point calculations including square root (see col. 17, line 40). The floating point system (see figure 4) appends a tag value (flag) to each floating point

number to indicate whether the corresponding floating point number is a normal floating point number or one of special floating point numbers (see abstract, lines 1-7). Lynch el al. further discloses in figure 6, the floating point system, in a process of a floating point operation, examining the tag value of an operand (138) to determining whether the operand is a special floating point number (140). Thus, the floating point system inherently includes a circuitry as an analyzer in order to examine tags values (see col. 18, line 58 through col. 19, line 9). Lynch et al. also discloses in figure 4 a register stack (84) for storing operand including result operand (see col. 15, line 22-23). Each operand is considered to include a register field (78) containing a floating point value, and a tag field (89) within the operand for storing an appending tag value as illustrated by the register stack (84) (see the bridging paragraph of cols. 15 and 16). It is noted that Lynch et al. does not explicitly disclose the resulting status tag being embedded with the resulting floating point operand. However, since Lynch et al. discloses in figure 6 a resulting tag value being generated for each operation result (steps 144), and in figure 4 the register stack (84) for storing operand including result operand having a tag field (89) within the operand for storing the a appending tag values (see the bridging paragraph of cols. 15 and 16), it would have been obvious to a person of ordinary skill in the art to store the floating point result with its tag as a resulting operand in the register stack (84) in order to quickly determine its status in subsequence operations. This would result in embedding the tag within the resulting floating point operand as claimed.

As per claims 2-4,15-17 and 27-29, the use of buffers for storing operand and intermediate results in a processing circuit is well known in the art to keep the logic level of

the operand from switching during processing. Therefore, including buffers in the floating point system of Lynch et al to keep the operand constant during analyzing and processing, if not inherent, would have been obvious to person of ordinary skill in the art in order to avoid error due to logic switching.

As per claim 6, Lynch et al also discloses the square root logic circuit organized according to the structure of a decision table (see col. 19, lines 6-8).

As per claim 7-13,19-29, and 31-37, Lynch et al. discloses in fig. 5 status of an operand.

(10) Response to Argument

In response to appellant's argument that the rejection does not make clear what portion of Lynch teaches the claimed status, the examiner respectfully submits that the rejection clearly set forth the tag value being the claimed status. As disclosed in Lynch et al. col. 18, lines 11-37, and figure 5 the tag value is clearly the same as the claimed status as it is to indicate whether the corresponding floating point number is a normal floating point number or one of special floating point numbers.

In response to appellant's argument that Lynch does not teach a result status embedded within the resulting operand, it is respectfully submitted that Lynch does suggest a resulting status embedded within the result operand in a square root operation. Lynch clearly discloses that the floating point unit (36) (see figure 4) appends a tag value to each floating point numbers, and stores the tag value with the floating point number in a register file (see abstract,

lines 1-7). As a result, an operand in the floating point unit is considered to be consisting of a floating point number with the appended tag. The floating point number is stored in the register field of the operand, and the tag values is stored in the tag field of the operand and within the operand as shown by the register stack (84) in which each register in the stack is to store an operand. Therefore, the tag value is clearly stored within the operand with the floating point number. Accordingly, as the floating point unit performs a square root operation in accordance with the flowchart in figure 6, the floating point unit would output a square root floating point result and a tag value that, as explained in the rejection, would be obviously to be appended to the floating point result, and stored within the result operand with the floating point result in a register of the register stack as claimed.

In response to appellant's argument that there is no motivation to modify Lynch to embed a result status with result operand, the examiner respectfully submitted that the rejection clearly provide a motivation to modify Lynch as to quickly determine the status of the result in subsequence operations. The motivation is base on the teaching in Lynch, column 3, lines 1-26

Finally, in response to appellant argument that the examiner has not provided any motivation to modify Lynch with buffers to store operand, it is respectfully submitted that the use of buffers for storing operand and intermediate results in a processing circuit is well known in the art to keep the logic level of the operand from switching during processing. Therefore, including buffers in the floating point system of Lynch et al to keep the operand constant during analyzing and processing, if not inherent, would have been obvious to person of

ordinary skill in the art in order to avoid error due to logic switching. The appellant also appears to presume the use of buffers in the floating point system to be well-known as the specification only mentions but does not disclose or explain the function of these buffers.

Therefore, it is respectfully submitted that the rejections are proper.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Chuong D Ngo
Primary Examiner

Conferees:

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

TUAN DAM
SUPERVISORY PATENT EXAMINER

SUN MICROSYSTEMS/FINNEGAN, HENDERSON LLP
901 NEW YORK AVENUE, NW
WASHINGTON,DC 20001-4413